IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Samson X. Huang

Title: REPAIRABLE MEMORY IN DISPLAY DEVICES

Docket No.: 884.326US1
Filed: September 28, 2000
Examiner: Fritz Alphonse

Serial No.: 09/675067
Due Date: April 2, 2004
Group Art Unit: 2675

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APPELLANTS' BRIEF ON APPEAL

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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For:	REPAIRABLE MEMORY IN DISPLAY DEVICES	)	
Assignee:	Intel Corporation		

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on 2 February 2004, from the Rejection of claims 1-25 of the above-identified application, as set forth in the Final Office Action dated 1 October 2003.

This Appeal Brief is filed in triplicate and accompanied by an authorization to charge the requisite fee set forth in 37 C.F.R. § 117(f) and any extension of time fee to Appellants' deposit account 19-0743. Appellants respectfully request reversal of the Examiner's rejection of pending claims

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, INTEL CORPORATION, a Delaware corporation doing business at 2625 Walsh Avenue, Santa Clara, CA 95051, in an assignment recorded on September 28, 2000 (Reel/Frame 011222/0240-0242).

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to the appellant which will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 1-25 are pending in the application and are rejected.

4. STATUS OF AMENDMENTS

No Amendment has been filed by the appellant subsequent to the Office Action dated October 1, 2003.

5. SUMMARY OF THE INVENTION

A system 200 according to an embodiment of the present invention comprises a memory 204 having a least significant bit and non-least significant bits. A repair router 202 in the system 200 utilizes the least significant bit to hold non-least significant information from any of the non-least significant bits.

6. ISSUES PRESENTED FOR REVIEW

I. Claims 1-6, 9-15, 20, and 24-25 were improperly rejected under 35 USC §102(b) as being anticipated by Nishikawa (U.S. Patent No. 5,805,604).

II. Claims 7-8, 16-19, and 21-23 were improperly rejected under 35 USC §103(a) as being unpatentable over Nishikawa (U.S. Patent No. 5,805,604) in view of Kondo (U.S. Patent No. 5,153,574).

7. GROUPING OF CLAIMS

Claims 1-6, 9-15, 20, and 24-25 stand together for purposes of this appeal.

Claims 7-8, 16-19, and 21-23 stand together for purposes of this appeal.

Appellant does not make any admission that any claim may not be argued in another forum as independently patentable from any other claim. Additionally, Appellant's grouping of claims above is provided for the purposes of this Appeal Brief only.

8. ARGUMENT

The Applicable Law: §102(b)

Claims 1-6, 9-15, 20, and 24-25 were rejected under 35 USC §102(b):

> "A person shall be entitled to a patent unless...the invention was patented or described in a printed publication in this or a foreign country....more than one year prior to the date of application for patent in the United States." 35 U.S.C. § 102(b).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick Co.*, 221

USPQ 481, 485 (Fed. Cir. 1984). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). "Inherent anticipation requires that the missing descriptive material is "necessarily present," not merely probably or possibly present, in the prior art." *Trintec Industries Inc. v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002).

The appellant respectfully submits that Nishikawa does not show all of the elements recited in claims 1-6, 9-15, 20, and 24-25 as required for anticipation according to this case law.

The Applicable Law: §103(a)

Claims 7-8, 16-19, and 21-23 were rejected under 35 USC §103(a):

> "A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a).

The MPEP states the following with regard to rejections under 35 USC § 103:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. " MPEP 2143.

A Federal Circuit opinion states that the suggestion or motivation to combine references and the reasonable expectation of success must both be found in the prior art. MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). The Federal Circuit has particularly emphasized the need for the PTO to furnish evidence in support of claim rejections under 35 USC § 103 in *In re Lee*:

> "When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness.....The factual inquiry whether to combine references must be thorough and

> searching....It must be based on objective evidence of record." *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

The appellant respectfully submits that the final Office Action has not shown all of the claim limitations in Nishikawa and Kondo, has not shown a sufficient suggestion or motivation to combine Nishikawa with Kondo, and has not shown a reasonable expectation of success of such a combination.

Rejections

I. The Rejection of Claims 1-6, 9-15, 20, and 24-25 under 35 USC §102(b).

Claims 1-6, 9-15, 20, and 24-25 were rejected under 35 USC §102(b) as being anticipated by Nishikawa. The appellant respectfully traverses.

Claims 1-6, 9-15, 20, and 24-25 stand together for purposes of this appeal. The appellant respectfully submits that Nishikawa does not show all of the elements recited in claims 1-6, 9-15, 20, and 24-25.

Independent claim 1 recites an apparatus comprising, among other elements, a first repair router having internal routing circuitry to route any of the plurality of non-least significant bits of the first repair router input data bus to the least significant bit of the memory device input data bus and to discard the least significant bit of the first repair router input data bus. Claims 2-6 and 24 are dependent on claim 1.

Independent claim 9 recites a memory device comprising, among other elements, routing circuitry to route any of a plurality of non-least significant bits of a repair router input data bus to the least significant bit of at least one of a plurality of addressable memory locations and to discard the least significant bit of the repair router input data bus. Claims 10-14 and 25 are dependent on claim 9.

Independent claim 15 recites a display system comprising, among other elements, a first repair router to utilize a least significant data bit of at least one of a plurality of addresses to hold

non-least significant information from any of a plurality of non-least significant data bits and to discard least significant information.

Independent claim 20 recites an integrated circuit comprising, among other elements, first and second repair routers wherein the first and second repair routers include internal routing circuitry to utilize a least significant bit of a first memory device as a non-least significant bit and to discard least significant information.

Nishikawa relates to an apparatus for reading and writing data including a rearranging circuit that rearranges bits of data having different significances when a region of a memory circuit has a defective portion. None of the bits in Nishikawa are discarded as is recited in all of the independent claims 1, 9, 15, and 20. This is shown by the following general quote from Nishikawa:

> "Embodiments in accordance with the present invention are effective to reduce the effect due to defects of a memory cell or a sector to a minimum, not by relieving a memory cell having a defect or avoiding a section having a defect, but by rearranging the data, in a memory circuit for storing image data and music data." Nishikawa, col 5, ln 58 to col 6, ln 2.

Specific embodiments of Nishikawa are described as follows:

> "Namely, when there is a defect in a part of a memory section 11, ... the rearranging circuit 12 rearranges respective bits representing image data, music data and the like so that a LSB (least significant bit) is stored in the defect region..... Therefore, when there is a defect in a region where an LSB is originally stored, there is no need to rearrange respective bits, but when there is a defect in a bit other than the LSB, for example, a region where a MSB (most significant bit) is stored, respective bits are rearranged so that the LSB is stored in the defect region." Nishikawa, col 6, ln 4-16.

> "In the first embodiment, when there exists a memory cell having a defect in any one region, the LSB is always stored in that region." Nishikawa, col 9, ln 61-63.

> "The rearranging circuit 12 rearranges data X7-X0 so that when a memory cell having a defect exists in a region to store a bit having large significance, such as the MSB, the LSB is stored in that region." Nishikawa, col 13, ln 6-10.

> "The rearranging circuit 12 rearranges data X15-X0 so that when a memory cell having a defect exists in a region to store a bit having greater significance on the MSB side of the 16 bits data, bits on the LSB side are stored in said region." Nishikawa, col 15, ln 63-67.

It is clear from these quotes that Nishikawa is not showing "each and every element as set forth in" independent claims 1, 9, 15, and 20, all of which recite discarding a least significant bit or least significant information. The final Office Action has not shown anticipation as defined by *Verdegaal Bros., Lindemann Maschinenfabrik,* and *Richardson v. Suzuki Motor* quoted above.

Neither has the final Office Action shown the claimed elements of discarding a least significant bit or least significant information as being inherent in Nishikawa. Indeed, one of the advantages according to Nishikawa is described:

> "Furthermore, since a circuit for blocking a memory cell having a defect portion or avoiding a sector having a defect is not required, the circuit size can be reduced." Nishikawa, col 17, ln 56-59.

Nishikawa is expressly stating that the missing descriptive material is not "necessarily present," not even "probably or possibly present," in Nishikawa. *Trintec Industries Inc.*

Claims 2-6, 10-14, and 24-25 are variously dependent on independent claims 1, 9, 15, and 20, and recite further limitations with respect to those claims. For reasons analogous to those stated above, and the recitations in the claims, the appellant respectfully submits that Nishikawa does not show all of the elements recited in claims 2-6, 10-14, and 24-25.

The appellant respectfully submits that Nishikawa does not show each and every element as set forth in claims 1-6, 9-15, 20, and 24-25. Reversal of the rejection of claims 1-6, 9-15, 20, and 24-25 under 35 USC §102(b) is respectfully requested.

II. The Rejection of claims 7-8, 16-19, and 21-23 under 35 U.S.C. §103.

Claims 7-8, 16-19, and 21-23 were rejected under 35 USC §103(a) as being unpatentable over Nishikawa in view of Kondo. The appellant respectfully traverses.

Claims 7-8, 16-19, and 21-23 stand together for purposes of this appeal.

Claims 7-8, 16-19, and 21-23 are variously dependent on independent claims 1, 9, 15, and 20, and recite further limitations with respect to those claims. As discussed above, Nishikawa does not show all of the elements recited in independent claims 1, 9, 15, and 20.

Kondo relates to an interface for a thin display panel having a timing circuit. Kondo, Abstract. Kondo describes the use of timing signals, and shows RAM memories with control circuits used to store color data. The final Office Action does not assert that Kondo contains the elements missing in Nishikawa. Therefore, the final Office Action has not shown that Nishikawa and Kondo together show or suggest all of the claimed features.

The final Office Action also does not identify a sufficient suggestion for combining Nishikawa with Kondo. The final Office Action states the following:

> "It would have been obvious to use the memory defect routing of Nishikawa in a LCD display system with three memory for color display. This would have been obvious as suggested by Nishikawa wherein Nishikawa's device is used for image data, "A rearranging circuit 12 has a function to rearrange respective bits representing image data...", col. 5, lines 40-41 of Nishikawa." Final Office Action, pages 4-5.

Although both Kondo and Nishikawa may store image data in memory devices, this is completely irrelevant to the technical combination proposed in the final Office Action, which involves memory defect routing. The end use that stored data is put to (an image in the instant case) has no bearing on how that data is stored in a memory device, and the method of storing the data does not affect the resulting image.

No suggestion or motivation for combining Kondo and Nishikawa can be found in the references themselves. Kondo does not describe the inner-workings of the RAM memories, and in particular does not describe how the RAM memories compensate for defective cells. RAM memories are commercially available, and the inner-workings of such a RAM memory does not need to be known for Kondo to have a complete description. The RAM memories in Kondo are "black boxes" with inputs and outputs. Although Nishikawa has stated that its methods can be used with a RAM memory, the final Office Action has not provided evidence that the inner-workings of the RAM memory shown in Kondo could be operated according to the method of Nishikawa. The final Office Action has not provided evidence that the RAM memory shown in Kondo does or does not have a method to compensate for defective cells. Therefore, there is no evidence of a suggestion for the technical combination set forth in the final Office Action. Given that Kondo does not discuss the inner-workings of the RAM memory devices, the final Office Action has also not shown evidence of a reasonable expectation of success of applying the method of Nishikawa to manage defective cells in the RAM memory devices of Kondo.

The final Office Action states:

> "Further, since Nishikawa is directed at providing a method and apparatus to mitigate memory defects without requiring the extra overhead of spare memory, it would have been obvious to include the rearranging circuits (i.e., rerouting circuitry) to the device of Kondo so as not to require extra memory and to require a change in the size of the memory. As combined, the system of Kondo and Nishikawa would simply add the input rearranging circuits 12 (first repair router) of Nishikawa to each of the inputs of memories 211, 212, and 213 of Kondo and add the output rearranging circuits 13 (second repair router) of Nishikawa on the outputs of memories 211, 212, and 213 of Kondo"..... "the use of a reflective electrode is well known in the art and would be obvious to use in a liquid crystal device without a back-light, i.e., these type of LCD displays are typical in watches or front lit displays." Final Office Action, page 5.

The final Office Action did not cite any evidence in Nishikawa or Kondo or any other prior art supporting the statements in the above-quoted paragraph as is required by *In re Vaeck* and *In re*

Lee. The final Office Action has not established a motivation to combine Nishikawa with Kondo, or a reasonable expectation of success, based on these statements.

The appellant respectfully submits that a *prima facie* case of obviousness of claims 7-8, 16-19, and 21-23 has not been established in the Office Action. Reversal of the rejection of claims 7-8, 16-19, and 21-23 under 35 U.S.C. §103 is respectfully requested.

9. REQUEST FOR REVERSAL

For the foregoing reasons, the appellant respectfully submits that the rejections of claims 1-6, 9-15, 20, and 24-25 under 35 USC §102(b), and claims 7-8, 16-19, and 21-23 under 35 U.S.C. §103, were erroneous. Reversal of those rejections is respectfully requested, as well as the allowance of all the rejected claims.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 1 April 2004 By _____
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Name KACIA LEE

Signature Kacia Lee

APPENDIX

The Claims on Appeal

1. (Previously Presented) An apparatus comprising:

a memory device having a memory device input data bus including a least significant bit and a plurality of non-least significant bits; and

a first repair router having a first repair router input data bus including a least significant bit and a plurality of non-least significant bits, and a first repair router output data bus coupled to the memory device input data bus, the first repair router having internal routing circuitry to route any of the plurality of non-least significant bits of the first repair router input data bus to the least significant bit of the memory device input data bus and to discard the least significant bit of the first repair router input data bus.

2. (Previously Presented) The apparatus of claim 1 wherein:

the plurality of non-least significant bits of the memory device input data bus includes a next-to-least significant bit; and

the first repair router further includes additional repair routing circuitry to route any of the non-least significant bits of the first repair router input data bus to the next-to-least significant bit of the memory device input data bus.

3. (Original) The apparatus of claim 1 wherein the memory device includes a memory device output data bus including a least significant bit and a plurality of non-least significant bits, the apparatus further comprising:

a second repair router having a second repair router input data bus coupled to the memory device output data bus, and having a second repair router output data bus including a least significant bit and a plurality of non-least significant bits, the second repair router having internal

routing circuitry to route the least significant bit of the memory device output data bus to any of the plurality of non-least significant bits of the second repair router output data bus.

4. (Original) The apparatus of claim 3 wherein the memory device includes a plurality of address ranges, and the first and second repair routers include address decoding circuitry to decode each of the plurality of address ranges.

5. (Original) The apparatus of claim 4 wherein the memory device includes two address ranges defined by a state of a most significant address bit.

6. (Original) The apparatus of claim 3 further comprising a display device coupled to the second repair router output data bus.

7. (Previously Presented) The apparatus of claim 6 wherein the display device is a color display device, and the memory device and first and second repair routers influence a first color of the color display device, the apparatus further comprising:

a second memory device; and

a second pair of repair routers coupled to the second memory device to influence a second color of the color display device.

8. (Previously Presented) The apparatus of claim 7 further comprising:

a third memory device; and

a third pair of repair routers coupled to the third memory device to influence a third color of the color display device.

9. (Previously Presented) A memory device comprising:

a plurality of addressable memory locations, each including a least significant bit and a plurality of non-least significant bits; and

a first repair router having a repair router input data bus with a least significant bit and a plurality of non-least significant bits, and having a repair router output data bus coupled to the plurality of addressable memory locations, the first repair router including routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the least significant bit of at least one of the plurality of addressable memory locations and to discard the least significant bit of the repair router input data bus.

10. (Original) The memory device of claim 9 wherein:

the plurality of addressable memory locations are arranged into a plurality of address ranges; and

the first repair router further includes address decoding circuitry to decode each of the plurality of address ranges.

11. (Original) The memory device of claim 10 further comprising a second repair router coupled to an output data bus of the memory device, the second repair router including routing circuitry to reverse any routing performed by the first repair router.

12. (Original) The memory device of claim 9 wherein the first repair router is configured to route a specific non-least significant bit to the least significant bit of the plurality of addressable memory locations when a problem exists with the specific non-least significant bit in at least one of the plurality of addressable memory locations.

13. (Original) The memory device of claim 9 further comprising a second repair router coupled to an output data bus of the memory device, the second repair router including routing circuitry to reverse any routing performed by the first repair router.

14. (Previously Presented) The memory device of claim 9 wherein:

the plurality of non-least significant bits of each of the addressable memory locations

includes a next-to-least significant bit; and

the first repair router further includes routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the next-to-least significant bit of at least one of the plurality of addressable memory locations.

15. (Previously Presented) A display system comprising:

a display device having an array of pixels;

a memory having a plurality of addresses, each of the plurality of addresses corresponding to one pixel in the array of pixels, and each of the plurality of addresses including a least significant data bit and a plurality of non-least significant data bits; and

a first repair router to utilize the least significant data bit of at least one of the plurality of addresses to hold non-least significant information from any of the plurality of non-least significant data bits and to discard least significant information.

16. (Original) The display system of claim 15 wherein the display device is a silicon light modulator.

17. (Original) The display system of claim 15 wherein the memory is configured to hold a first color information, the display system further comprising:

a second memory configured to hold second color information; and

a second repair router coupled to the second memory.

18. (Original) The display system of claim 17 further comprising:

a third memory configured to hold third color information; and

a third repair router coupled to the third memory.

19. (Previously Presented) The display system of claim 15 wherein:

the plurality of addresses are arranged in a plurality of groups; and

the first repair router includes routing circuitry to utilize the least significant bits of each of the plurality of groups separately.

20. (Previously Presented) An integrated circuit comprising:

a first memory device having an input data bus and an output data bus;

first and second repair routers coupled to the input data bus and the output data bus, respectively, the first and second repair routers including routing circuitry to route data to and from the first memory device as a function of defects in the first memory device; and

wherein the first and second repair routers include internal routing circuitry to utilize a least significant bit of the first memory device as a non-least significant bit and to discard least significant information.

21. (Previously Presented) The integrated circuit of claim 20 further comprising a reflective electrode coupled to the first memory device, the reflective electrode having a plurality of pixels responsive to data from the first memory device as received by the second repair router.

22. (Previously Presented) The integrated circuit of claim 21 wherein:

the first memory device includes a plurality of groups of data locations; and

the first and second repair routers each include circuitry to separately route data for each of the plurality of groups of data locations.

23. (Original) The integrated circuit of claim 22 further comprising:

second and third memory devices; and

second and third pairs of repair routers coupled to the second and th ird memory devices respectively.

24. (Previously Presented) The apparatus of claim 2 wherein:

the first repair router further includes additional repair routing circuitry to discard a next-to-least significant bit of the first repair router input data bus.

25. (Previously Presented) The memory device of claim 14 wherein:

the first repair router further includes routing circuitry to discard a next-to-least significant bit of the repair router input data bus.